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(54) SILICON SINGLE CRYSTAL WAFER WITH LOW CONTENT OF CRYSTAL DEFECT AND ITS PRODUCTION

(57)Abstract:

PROBLEM TO BE SOLVED: To produce a silicon single crystal wafer having a wide control width and an ultralow defect density over the whole surface of the crystal in the absence of both a V-rich region and an I-rich region under readily controllable production conditions by specifying the pulling up conditions of the crystal when growing the silicon single crystal according to a Czochralski (CZ) process.

SOLUTION: A crystal is pulled up in a region surrounded by a border line between a V-rich region and an N-region and a border line between the N-region and an I-rich region in a defect distribution chart indicating the defect distribution for the distance D (mm) from the crystal center to the periphery of the crystal as the abscissa axis versus a value of F/G (mm2/°C.min) as the ordinate axis when the pulling up speed is F (mm/min) and the average value of the gradient of the temperature in the crystal in the pulling up axis direction in a region of temperatures from the melting point of the silicon to 1,400°C is expressed as G (°C/mm). The value of F/G is preferably regulated to 0.112-0.142 mm2/° C.min at the crystal center to pull up the crystal.

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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The silicon single crystal wafer characterized by for the nucleus of the OSF ring generated in the shape of a ring or an OSF ring existing in the silicon single crystal wafer raised by the Czochrlski method when thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface.
[Claim 2] It is the silicon single crystal wafer characterized by not generating an OSF ring and FPD and ratio of length to diameter not existing in the whole wafer surface when OSF thermal oxidation processing is carried out although the oxygen density of the whole wafer surface is less than 24 ppmas and the potential nucleus of an OSF ring exists by oxygen precipitation heat treatment in the silicon single crystal wafer raised by the Czochrlski method.
[Claim 3] In case a silicon single crystal is raised with the Czochrlski method, a pull-up rate is set to F [mm/min]. When the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], In the defective distribution map in which having set the axis of abscissa as the distance D from a crystal center to the crystal circumference [mm], and having shown defective distribution by setting an axis of ordinate as the value of F/G [mm2 / **, and min] The manufacture approach of the silicon single crystal wafer characterized by pulling up a crystal in the field surrounded by the borderline of a V-rich field and N-field, and the borderline of N-field and an I-rich field.
[Claim 4] The manufacture approach of the silicon single crystal wafer indicated to claim 3 characterized by pulling up a crystal for the value of said F/G as 0.112-0.142mm2/degree C and min in a crystal center.
[Claim 5] The manufacture approach of the silicon single crystal wafer indicated to claim 3 or claim 4 characterized by controlling so that the time amount which passes through the temperature region from 1050 degrees C to 850 degrees C under said crystal becomes 140 or less minutes.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a silicon single crystal wafer with few crystal defects, and its manufacture approach.
[0002]
[Description of the Prior Art] In recent years, the quality demand to the silicon single crystal produced with the Czochrlski method (it is hereafter written as a CZ process) used as the substrate has been increasing with detailed-izing of the component accompanying high integration of a semiconductor circuit. The defect of a single crystal growth reason in which the oxide film proof-pressure property especially called grown-in (Grown-in) defects, such as FPD, LSTD, and COP, and the property of a device are worsened exists, and importance is attached to reduction of the consistency and size.
[0003] In explaining these defects, it explains being known generally about the factor which determines each concentration of the point defect of the hole mold first called the Vacancy (it may outline Vacancy and Following V) incorporated by the silicon single crystal, and the mold silicon point defect between grids called Interstitial-Si (it may outline Interstitial-Si and Following I) incorporated.
[0004] In a silicon single crystal, V fields are Vacancy, i.e., the crevice generated from lack of a silicon atom, and a field with many things like a hole. With an I region It is the thing of a field with many lumps of the rearrangement and the excessive silicon atom which are generated when a silicon atom exists in an excess. Between V field and an I region The neutral (it may outline Neutral and Following N) field without lack of an atom or an excess (few) will exist. And with [even if said grown-in defects (FPD, LSTD, COP, etc.) occur when V and I are in a condition / ****** / to the last, and it has the bias of some atoms] saturation [below], it has turned out that it does not exist as a defect.
[0005] The concentration of both this point defect is decided from the pull-up rate (growth rate) of the crystal in a CZ process, and relation with the temperature gradient G near [under crystal] the solid-liquid interface, and existence of the defect of the shape of a ring called OSF (an oxidation induction stacking fault, Oxidation Indused Stacking Fault) is checked in the boundary neighborhood of V field and an I region.
[0006] A classification of the defect of these crystal growth reason calls the V-rich field the field where grown-in defects by which it is considered as the void reason to which hole type point defects gathered when a growth rate is a high speed comparatively, the above before and after 0.6 mm/min and, such as FPD, LSTD, and COP, exist in high density throughout the direction of the diameter of a crystal, and these defects exist (refer to drawing 4 (a)). Moreover, when a growth rate is 0.6 or less mm/min, the field where the above-mentioned OSF ring is generated from the circumference of a crystal with lowering of a growth rate, the defect of ratios of length to diameter (Large Dislocation: the code of the dislocation loop between grids, LSEPD, LFPD, etc.) considered to be dislocation loop reasons by the outside of this ring exists in a low consistency, and these defects exist is called the I-rich field (refer to drawing 4 (b)). Furthermore, if a growth rate is made into a low speed 0.4 mm/min order, an OSF ring will condense and disappear at the core of a wafer, and the whole surface will serve as an I-rich field (drawing 4 (c)).
[0007] Moreover, the existence of the field where neither FPD of a hole reason, LSTD, COP nor LSEPD of a dislocation loop reason and LFPD exist called N field to the outside of an OSF ring is discovered in the medium of a V-rich field and an I-rich field recently (refer to JP,8-330316,A). It is reported that this field is the I-rich field side which is not so rich as there is almost no precipitation of oxygen by being in the outside of an OSF

ring when oxygen precipitation heat treatment is performed and the contrast of a deposit is checked by X-ray observation etc., and LSEPD and LFPD are formed (refer to drawing 3 (a)). And improve the temperature distribution in furnace of a pull-up machine for N field which exists only in the pole of a wafer part in the conventional CZ pull-up machine, and a pull-up rate is adjusted. F/G value (when setting a crystal pulling rate to F [mm/min] and setting the average of inclination to G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1300 degrees C]) If it controls to the whole wafer surface and a crystal overall length by setting to 0.20-0.22mm2 / **, and min the ratio expressed with F/G, it will be proposed that it is possible to extend N field all over a wafer (refer to drawing 3 (b)).

[0008]
[Problem(s) to be Solved by the Invention] However, if it is going to extend and manufacture such a super-low defective field into the whole crystal, since this field will be limited only to N field by the side of an I-rich field, if it is an experimental aircraft, it is [with a production machine, / precision control is difficult and / a difficulty] in productivity at any rate, and is not practical [a control range is very narrow on manufacture conditions, and]. Furthermore, it became clear that it differed from the created defective distribution map (refer to drawing 1) based on the data for which this invention persons experimented and investigated the defective distribution map currently indicated by this invention, and it asked, and data substantially.

[0009] This invention was made in view of such a trouble, and its control width of face is wide, and it aims at obtaining the silicon single crystal wafer by the CZ process which is super-low defect density, maintaining high productivity under the manufacture conditions which are easy to control by continuing all over the crystal with which neither a V-rich field nor an I-rich field exists.

[0010]
[Means for Solving the Problem] Invention which it was accomplished in order that this invention might attain said object, and was indicated to claim 1 of this invention is a silicon single crystal wafer characterized by for the nucleus of the OSF ring generated in the shape of a ring or an OSF ring existing when thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface in the silicon single crystal wafer raised by the CZ process.

[0011] and as the manufacture approach of such a silicon single crystal wafer As indicated to claim 3 of this invention, in case a silicon single crystal is raised with the Czochrlski method When a pull-up rate is set to F [mm/min] and the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], In the defective distribution map in which having set the axis of abscissa as the distance D from a crystal center to the crystal circumference [mm], and having shown defective distribution by setting an axis of ordinate as the value of F/G [mm2 / **, and min] It is the manufacture approach of the silicon single crystal wafer characterized by pulling up a crystal in the field surrounded by the borderline of a V-rich field and N-field, and the borderline of N-field and an I-rich field.

[0012] Thus, so that it may be settled in the field surrounded by the borderline of a V-rich field and N-field, and the borderline of N-field and an I-rich field based on the defective distribution map of drawing 1 which analyzed and searched for the result of an experiment and examination If the average G of inclination is controlled from the pull-up rate F of a crystal, and the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C] and a crystal is pulled up The silicon single crystal wafer with which the nucleus of the OSF ring generated in the shape of a ring or an OSF ring exists when thermal oxidation processing indicated to said claim 1 is carried out, and FPD and ratio of length to diameter do not exist in the whole wafer surface is producible.

[0013] Furthermore, it is in a concrete target. We are a crystal center about the value of said F/G, and decided to pull up a crystal as 0.112-0.142mm2 / **, and min (claim 4).

[0014] Thus, although the field which may generate an OSF ring at the time of thermal oxidation processing has been included so that drawing 1 may see by controlling the value of F/G by the crystal center to 0.112-0.142mm2 / **, and min Since N field of OSF ring inside and outside is pulled up as the maximum amplification is carried out, a control range with inclination becomes large a pull-up rate and whenever [crystal internal temperature], manufacture conditioning becomes easy also in a production machine, and a wafer with many N fields can be produced easily.

[0015] Thus, although an OSF ring is generated in the shape of a ring or the nucleus of an OSF ring is latent

when the silicon single crystal wafer obtained by the manufacture approach of this invention according to claim 3 or 4 carries out thermal oxidation processing for this wafer It is the wafer of not existing in the whole wafer surface, and all over the so-called wafer, a V-rich field and an I-rich field do not exist but FPD and ratio of length to diameter (LSEPD, LFPD) have an area of neutrality N field very big [a field], as shown in <u>drawing 2</u> (b). It is the wafer which had the new defect structure which expanded N field of said OSF ring outside, and N field of the OSF ring inside to the maximum in the silicon wafer of large this invention of such an N field using N field existing also inside the OSF ring which OSF may generate in the shape of a ring when the nucleus of an OSF ring is latent and thermal oxidation processing of this wafer is carried out.

[0016] And in the silicon single crystal wafer with which invention indicated to claim 2 of this invention was raised by the CZ process, although the oxygen densities of the whole wafer surface are under 24ppma(s) (ASTM'79 value) and, as for the potential nucleus of an OSF ring, exist by oxygen precipitation heat treatment, it is the silicon single crystal wafer characterized by not generating an OSF ring when OSF thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface. And it was made to control as the manufacture approach of such a silicon single crystal wafer, in addition to the manufacture approach indicated to claim 3 or claim 4, so that the time amount which passes through the temperature region from 1050 degrees C to 850 degrees C under said crystal becomes 140 or less minutes as indicated to claim 5 of this invention.

[0017] Thus, if the heat history is controlled as it has been 140 or less minutes about the time amount which holds down the oxygen density in a growth crystal to less than 24 ppmas, or passes through the temperature region from 1050 degrees C to 850 degrees C under growth crystal Since a device is not affected even if it can check growth of an OSF nucleus and the potential nucleus of an OSF ring or an OSF ring exists in a wafer on parenchyma, although the nucleus of an OSF ring is latent when OSF thermal oxidation processing is carried out, after all this wafer An OSF ring is not generated and they are FPD and ratio of length to diameter (it LSEPD(s)). the whole surface where neither LFPD nor an OSF ring with which the so-called whole wafer surface does damage also for a V-rich field and an I-rich field of not existing in the whole wafer surface exists -- it can continue all over an usable crystal and a wafer [defect density super-low] can be obtained. And it is possible to also make control of F/G into a large control range in this case, and a wafer can be produced easily practically.

[0018] Hereafter, although explained to a detail per this invention, this invention is not limited to these. In advance of explanation, lessons is taken from each vocabulary, and it explains beforehand.

1) K2 Cr 2O7 after cutting down a wafer from the silicon single crystal rod after growth and etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid in FPD (Flow Pattern Defect) A pit and a ripple pattern arise by etching a front face with the mixed liquor of fluoric acid and water (Secco etching). This ripple pattern is called FPD, and the defects of oxide-film pressure-proofing increase in number, so that the FPD consistency within a wafer side is high (refer to JP,4-192345,A).

[0019] 2) When the same Secco etching as FPD is performed, call SEPD (Secco Etch Pit Defect) a thing without FPD, a call, and a flow pattern for the thing accompanied by a flow pattern (flow pattern) with SEPD. When it is thought in this that large SEPD (LSEPD) 10 micrometers or more originates in a rearrangement cluster and a rearrangement cluster exists in a device, a current leaks through this rearrangement and it stops achieving the function as a P-N junction.

[0020] 3) Cut down a wafer from the silicon single crystal rod after growth, and carry out cleavage of the wafer to LSTD (Laser Scattering Tomography Defect) after etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid. Incidence of the infrared light can be carried out from this cleavage plane, and the scattered light by the defect which exists in a wafer can be detected by detecting the light which came out from the wafer front face. About the scatterer observed here, it is an institute etc., there is already a report, and it is regarded as the oxygen sludge (J. J.A.P. Vol.32, P3679, 1993 reference). Moreover, the result that it is the void (hole) of octahedron is also reported by the latest research.

[0021] 4) the defect which becomes the cause of degrading oxide film pressure-proofing of the core of a wafer, with COP (Crystal Originated Particle) -- it is -- Secco -- by SC-1 washing (washing by the mixed liquor of NH4 OH:H2 O2:H2 O=1:1:10), the defect set to FPD if dirty works as a selection etching reagent, and is set to COP. The diameter of this pit is investigated with light scattering measurement by 1 micrometer or less.

[0022] 5) It is the defect which there are LSEPD, LFPD, etc. in ratio of length to diameter (Large Dislocation:

code of the dislocation loop between grids), and is considered to be a dislocation loop reason. A large thing 10 micrometers or more is said that LSEPD described above also in SEPD. Moreover, also in FPD which LFPD described above, the magnitude of a head pit says a large thing 10 micrometers or more, and it is considered the dislocation loop reason also here.

[0023] the place investigated in the detail about the boundary neighborhood of V field and an I region about the silicon single crystal growth by the CZ process as this invention persons proposed by Japanese Patent Application No. No. 199415 [nine to] previously -- **** of this boundary neighborhood -- the narrow field had few FPD(s), LSTD(s), and COP remarkably, and it discovered that there was a neutral field where LSEPD does not exist, either.

[0024] Then, if this neutral field can be extended all over a wafer, it will conceive that a point defect can be reduced substantially, and since the pull-up rate is almost fixed in the wafer side of a crystal, the main factors which determine concentration distribution of the point defect within a field will be temperature gradients in a growth (pull-up) rate and the relation of a temperature gradient. That a difference is in the temperature gradient of shaft orientations in a wafer side that is, on a problem If this difference can be reduced, that the concentration difference of the point defect within a wafer side can also be reduced A header, When controlling whenever [furnace temperature] and adjusting the pull-up rate so that the difference of the temperature gradient Gc of the crystal center section and the temperature gradient germanium of a crystal circumference part might be set to **G=(germanium-Gc) <=5 degree-C/cm, a wafer without the defect which the whole wafer surface becomes from N field came to be obtained.

[0025] In this invention, as a result of difference **G of the above temperature gradients using the crystal pulling equipment by the small CZ process, changing a pull-up rate and investigating the inside of the crystal face, the following knowledge was newly acquired. Although N field which exists between a V-rich field and an I-rich field was conventionally considered to be only the outside of an OSF ring (nucleus), it checked that N field existed also inside an OSF ring (refer to drawing 2 (a)). namely, the case of above-mentioned Japanese Patent Application No. No. 199415 [nine to] -- an OSF ring -- a V-rich field and the border area of N field -- becoming -- **** (refer to drawing 3 (a)) -- it turned out that these two are not necessarily in agreement. This is not discovered when it experiments with the large crystal pulling equipment of the conventional **G, but as a result of investigating the crystal which used the small crystal pulling equipment of the **G above-mentioned this time, it is discovered.

[0026] Whenever [furnace temperature / of the pull-up equipment in this examination] was wholeheartedly analyzed using the comprehensive heat transfer analysis software FEMAG (F. 33 Dupret, P.Nicodeme, Y.Ryckmans, P.Wouters, and M.J.Crochet, Int.J.Heat MassTransfer, 1849 (1990)). When a pull-up rate is set to F [mm/min] and the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], the value of F/G consequently, in a crystal center If the pull-up rate F and the temperature gradient average G are controlled to become within the limits of 0.112-0.142mm2 / **, and min Although the nucleus of the OSF ring generated in the shape of a ring or an OSF ring existed when OSF thermal oxidation processing was carried out, it turned out that the silicon single crystal wafer with which FPD and ratio of length to diameter do not exist in the whole wafer surface is obtained.

[0027] Although drawing 1 is the case where a silicon single crystal with a diameter of 6 inches is made into an example, it expresses many defective distribution at the time of setting an axis of abscissa as the direction location of a path of a crystal, and setting an axis of ordinate as F/G value. Between a crystal center location and the location from a core to about 50mm, the boundary of a V-rich field / N field goes up gently from 0.142mm2 / **, and min, and if it applies to a periphery from this location, it is on the line which increased F/G value rapidly, so that clearly from drawing 1 . The cores of an OSF ring field are about 0.125mm2 / **, and min, and if it applies to a crystal periphery, they are on the line which increased F/G value rapidly almost in parallel with the borderline of a V-rich field / N field. Furthermore, the boundary with N field / I-rich field was set to 0.112mm2 / **, and min between the crystal center location and the location from a core to about 70mm, and has fallen rapidly toward the crystal periphery after that. Therefore, what is necessary is just to make it become 0.112-0.142mm2 / **, and min in a crystal center location, in order to make the most of N field in the wafer containing an OSF ring.

[0028] When this was explained in respect of the wafer, as it was conventionally shown in drawing 3 (a)

Although a pull-up rate and **G tended to be controlled using special crystal pulling equipment and it was going to manufacture the defect-free crystal that N field which exists in the outside of the OSF ring in a usual pull-up rate and crystal pulling equipment should be expanded all over a crystal (refer to drawing 3 (b)) Control was difficult, and the control width of face of manufacture conditions, such as a pull-up rate and a temperature gradient, is very narrow, and it was not [the difficulty was in productivity and] practical.

[0029] In this invention, it did not limit only to N field of the outside of an OSF ring, but N field was made to carry out the maximum amplification also using N field (refer to drawing 2 (a)) which exists also inside the OSF ring discovered this time. That is, the pull-up rate, **G, and crystal pulling equipment to which N field can be expanded all over the maximum wafer while the OSF ring had been included, as shown in drawing 2 (b) were chosen and pulled up. Consequently, if inclination is adjusted and pulled up a pull-up rate and whenever [crystal internal temperature] so that it may fall within the range of F/G value which was described above, the wafer of a low defect can be easily manufactured under manufacture conditions with the control width of face expanded conventionally.

[0030] It turns out that an OSF ring is not generated by thermal oxidation processing even if the nucleus of an OSF ring exists in the whole wafer surface from the latest research in the case of hypoxia concentration, and a device is not affected about an OSF ring on the other hand. If the oxygen density in the whole wafer surface is less than 24 ppmas as a result of using the same crystal pulling equipment for the threshold value of this oxygen density and pulling up the crystal of some kinds of oxygen density level, when thermal oxidation processing of a wafer is performed, it is checked that an OSF ring is not generated.

[0031] That is, although it is to 24ppma(s) that the nucleus which serves as OSF covering a crystal overall length exists when drawing 5 lowers an oxygen density gradually while raising the crystal of one, but an OSF ring is observed when thermal oxidation processing of a wafer is performed and an OSF ring nucleus exists in less than 24 ppmas, it means that the OSF ring by thermal oxidation processing is not generated.

[0032] Incidentally, in order to set the oxygen density under growth crystal to less than 24 ppmas, that what is necessary is just to carry out by the approach generally used from the former, distribution etc. can be adjusted whenever [rotational frequency / of a crucible /, or melt internal temperature], and the means of controlling the convection current of melt can perform easily.

[0033] In addition, even if an OSF ring is not generated, there is an inclination for precipitation of oxygen to decrease, in the place where the nucleus exists, but since strong gettering is not required in the bottom process of low temperature of a device, either, the little of the precipitation of oxygen in an OSF field does not become a problem.

[0034] Subsequently, the conditions which check growth of an OSF ring nucleus were examined. So that some kinds of crystal pulling equipments (what changed the configuration in a furnace) with which temperature distribution in furnace differs may be used and an OSF ring may be generated at the time of OSF thermal oxidation processing Into the crystal which gave the heat history which passes through a 1050-850-degree C temperature band in 140 or less minutes as a result of controlling a pull-up rate and pulling up a crystal OSF thermal oxidation processing in which the existence of OSF ring generating is checked after that is performed. The ** OSF ring was not checked (I.). [Yamashita] and Y.Shimanuki:The Electrochemical SocietyExtended Abstract and Los Angels, Carifornia, and May7- 12, 1989, and P.346 reference.

[0035] Then, in addition to F / G value control, an oxygen density is held down to less than 24 ppmas during a crystal. Or if the heat history which passes through the temperature region from 1050 degrees C to 850 degrees C of a growth crystal is controlled as it has been 140 or less minutes, and growth of an OSF ring nucleus is checked When OSF thermal oxidation processing is carried out, there is nothing, FPD and ratio of length to diameter do not exist, but the whole crystal surface is occupied in an usable field, and generating of an OSF ring can produce a defect-free crystal in the large condition range.

[0036] Namely, in case a silicon single crystal is raised by the CZ process, a pull-up rate is set to F [mm/min]. When the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], the value of F/G in a crystal center Control to 0.112-0.142mm2 / **, and min, and an oxygen density is held down to less than 24 ppmas during a crystal. Or by controlling so that the time amount which passes through the temperature region from 1050 degrees C to 850 degrees C under said crystal becomes 140 or less minutes the whole surface which an OSF ring does not generate even if it carries out thermal oxidation processing, while having large N field --

an usable defect-free wafer can be easily manufactured under the conditions that control width of face is wide.
[0037]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail, referring to a drawing. First, drawing 6 R> 6 explains the example of a configuration of the crystal pulling equipment by the CZ process used by this invention. As shown in drawing 6 , this crystal pulling equipment 30 The pull-up room 31, the crucible 32 prepared all over the pull-up room 31, and the heater 34 arranged around a crucible 32, It has the reel style (not shown) which rotates or rolls round the crucible maintenance shaft 33 made to rotate a crucible 32 and its rolling mechanism (not shown), the seed chuck 6 holding the seed crystal 5 of silicon, the cable 7 that pulls up a seed chuck 6, and a cable 7, and is constituted. A quartz crucible is prepared in the side in which a crucible 32 holds the silicon melt (molten bath) 2 of the inside, and the graphite crucible is prepared in the outside. Moreover, the heat insulator 35 is arranged around [outside] the heater 34.
[0038] Moreover, in order to set up the manufacture conditions in connection with the manufacture approach of this invention, the annular solid-liquid interface heat insulator 8 is formed in the periphery of the solid-liquid interface of a crystal, and the up surrounding heat insulator 9 is arranged on it. This solid-liquid interface heat insulator 8 forms the 3-5cm clearance 10 between that soffit and surface of hot water of silicon melt 2, and is installed in it. The up surrounding heat insulator 9 may not be used depending on conditions. Furthermore, coolant gas is sprayed or the tubed cooling system 36 which interrupts radiant heat and cools a single crystal is formed. Independently, by installing the magnet which is not illustrated in the horizontal outside of the pull-up room 31, and impressing magnetic fields, such as a horizontal direction or a perpendicular direction, to silicon melt 2, the convection current of melt is controlled and, recently, the so-called MCZ method for measuring the stable growth of a single crystal is used in many cases.
[0039] Next, the single-crystal-growth approach by above crystal pulling equipment 30 is explained. First, within a crucible 32, the high grade polycrystal raw material of silicon is heated more than the melting point (about 1420-degreeC), and is dissolved. Next, the head of a seed crystal 5 is made contacted or immersed in the surface abbreviation core of melt 2 by beginning to roll a cable 7. Then, while rotating the crucible maintenance shaft 33 in the proper direction, single crystal growth is started by rolling round rotating a cable 7 and pulling up a seed crystal 5. Henceforth, the single crystal rod 1 of an approximate circle column configuration can be obtained by adjusting a pull-up rate and temperature appropriately.
[0040] In this case, in this invention, especially in order to attain the object of this invention, as shown in drawing 6 , in the periphery space of the liquefied part in the single crystal rod 1 on the surface of hot water of the pull-up room 31, it is important that the temperature of the crystal near the surface of hot water formed the annular solid-liquid interface heat insulator 8 in the temperature region from 1420 degrees C to 1400 degrees C and to have arranged the up surrounding heat insulator 9 on it. Furthermore, it is good also as structure which should form the equipment 36 which cools a crystal, for example, a cooling system, in the upper part of this heat insulator if needed, should spray coolant gas on this from the upper part, should cool the crystal, and attached the radiant heat reflecting plate in the cylinder lower part.
[0041] Thus, since a heat insulation effect is acquired by radiant heat near the crystal growth interface and the radiant heat from a heater etc. can be cut in the upper part of a crystal by establishing a predetermined clearance in the location of the right above of an oil level, arranging a heat insulator, and considering as the structure which formed further the equipment which cools a crystal in the upper part of this heat insulator, the manufacture conditions of this invention can be satisfied. An air-cooling duct, a water-cooled coil, etc. which surround the perimeter of a crystal are formed, and you may make it secure a desired temperature gradient independently [said tubed cooling system 36] as a cooling system of this crystal.
[0042] Conventional equipment was shown in drawing 7 for the crystal pulling equipment used by this invention, and a comparison. Although it is the same as the pull-up equipment used by this invention about fundamental structure, neither the solid-liquid interface heat insulator 8, the up surrounding heat insulator 9 nor the cooling system 36 is equipped.
[0043]
[Example] Although an example is given and the gestalt of concrete operation of this invention is explained hereafter, this invention is not limited to these.
(Example 1) It raised, having charged 60kg of raw material polycrystalline silicon to the 20 inch quartz crucible, and lowering an average pull-up rate for the diameter of 6 inches, and the silicon single crystal rod of

bearing <100> to 0.88 - 0.50 mm/min with the pull-up equipment 30 shown in drawing 6 , (body die length of about 85cm of a single crystal rod). It was made into 4cm space from about 1420 degrees C and the surface of hot water up to the soffit of an annular solid-liquid interface heat insulator, on it, the water temperature of silicon melt has arranged the annular solid-liquid interface heat insulator of 10cm height, it adjusted the crucible maintenance shaft, set the height from the surface of hot water to pull-up room head lining as 30cm, and arranged the up surrounding heat insulator. And F/G value in the crystal center section were changed to 0.22-0.10mm2 and **/min, and was pulled up.

[0044] From the single crystal rod obtained here, the wafer was cut down, mirror plane processing was performed, the mirror plane wafer of a silicon single crystal was produced, and the grown-in defect was measured. Moreover, thermal oxidation processing was performed and the existence of OSF ring generating was checked. Consequently, although the OSF ring field which F/G value generates from the wafer periphery section in about 15mm location at the time of thermal oxidation processing within the limits of 0.112-0.142mm2 / **, and min existed, the super-low defective wafer which carried out the maximum amplification of the N field where the grown-in defect of these ring inside and outside does not exist was obtained. In addition, the oxide-film proof-pressure property of this wafer became 100% of rates of C-mode excellent article. In addition, the C-mode Measuring condition is as follows.

1) Oxide-film thickness : 25nm Two measuring electrode: Phosphorus dope polish recon 3 electrode-surface product: 8mm2 4 judging current: 1 mA/cm2 5 excellent-article judging: Dielectric-breakdown electric field judged the thing of 8 or more MV/cm to be an excellent article.

[0045] (Example 2) Except having carried out by lowering an oxygen density gradually during crystal pulling, it raised on the same conditions as an example 1, and from the obtained single crystal rod, the wafer was cut down, mirror plane processing was performed, the mirror plane wafer of a silicon single crystal was produced, and the grown-in defect was measured. Moreover, thermal oxidation processing was performed and the existence of OSF ring generating was checked.

[0046] Consequently, F/G value of the wafer of 24 or more ppmas was the super-low defective wafers with which the oxygen density within a wafer side has an OSF ring from a wafer core in N field in which a whole surface grown-in defect does not exist in about 15mm location within the limits of 0.112-0.142mm2 / **, and min. On the other hand, the oxygen density within a wafer side was the defect-free wafer which does not generate an OSF ring by thermal oxidation processing, although the OSF nucleus existed in N field in which, as for the wafer of less than 24 ppmas, a whole surface grown-in defect does not exist. In addition, the oxide-film proof-pressure property of this wafer became 100% of rates of C-mode excellent article.

[0047] (Example 3) Except having given the heat history which made time amount which passes through the temperature region to 1050-850 degrees C under crystal 140 or less minutes during crystal pulling, it raised on the same conditions as an example 1, and from the obtained single crystal rod, the wafer was cut down, mirror plane processing was performed, the mirror plane wafer of a silicon single crystal was produced, and the grown-in defect was measured. Moreover, thermal oxidation processing was performed and the existence of OSF ring generating was checked.

[0048] Consequently, even if the oxygen density was the thing of 27ppma(s), F/G value was the defect-free wafers which do not generate an OSF ring by thermal oxidation processing, although the OSF nucleus existed in N field in which a whole surface grown-in defect does not exist within the limits of 0.112-0.142mm2 / **, and min. In addition, the oxide-film proof-pressure property of this wafer became 100% of rates of C-mode excellent article.

[0049] In addition, this invention is not limited to the above-mentioned operation gestalt. The above-mentioned operation gestalt is instantiation, and no matter it may be what thing which has the same configuration substantially with the technical thought indicated by the claim of this invention, and does the same operation effectiveness so, it is included by the technical range of this invention.

[0050] For example, although the example was given and explained per in the above-mentioned operation gestalt when a silicon single crystal with a diameter of 6 inches was raised When this invention is not limited to this, but a pull-up rate is set to F [mm/min] and the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], the value of F/G in a crystal center If it controls to be set to 0.112-0.142mm2 / **, and min, it is applicable also to the diameter of 8-16 inches, or the silicon single crystal beyond it. Moreover, it cannot be

overemphasized that this invention is applicable also to the so-called MCZ method for impressing a level magnetic field and length magnetic field, a cusp field, etc. to silicon melt.
[0051] Furthermore, in the above-mentioned operation gestalt, although hypoxia-izing and heat history control were explained independently, both both may be carried out and an OSF ring can be defanged more certainly.
[0052]
[Effect of the Invention] As explained above, according to this invention, the control width of face of single-crystal-growth conditions becomes large, and the wafer to which the maximum N field was expanded can be easily produced by using N field of an OSF ring outside, an OSF ring or an OSF nucleus, and N field of the inside. And if hypoxia-izing or control of the heat history of a low temperature range is used together, an OSF ring will not be generated, either, but a glow in defect can also manufacture a silicon single crystal wafer with the defect-free whole wafer surface of super-low level.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.


DRAWINGS

[Drawing 1]
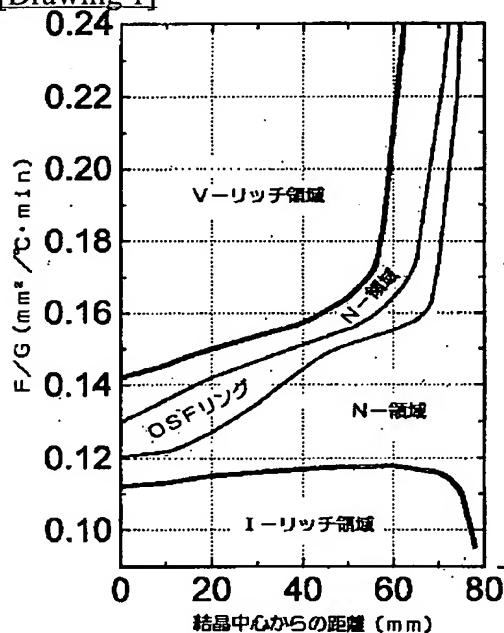
[Drawing 2]

[Drawing 3]

[Drawing 4]

(a)　　　　　　(b)　　　　　　(c)

[Drawing 6]

[Drawing 5]

(a)　　　　　　　　　　　　　(b)

酸素（O1）濃度 [ppma]

結晶長さ [cm]

OSFリング

OSF核
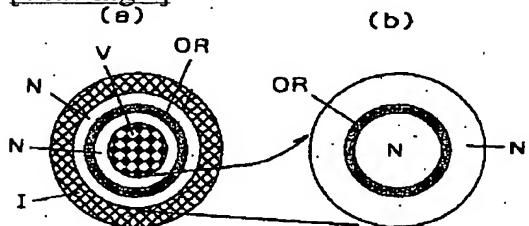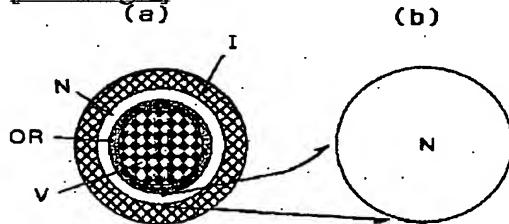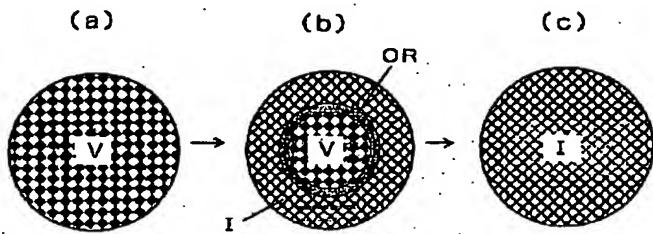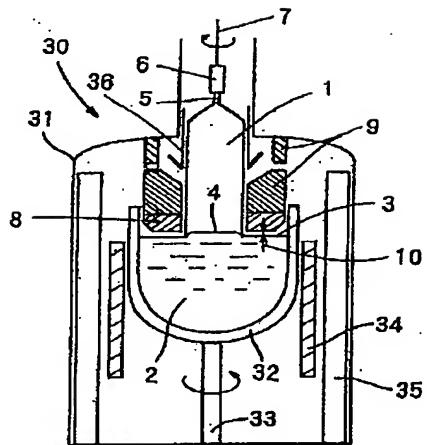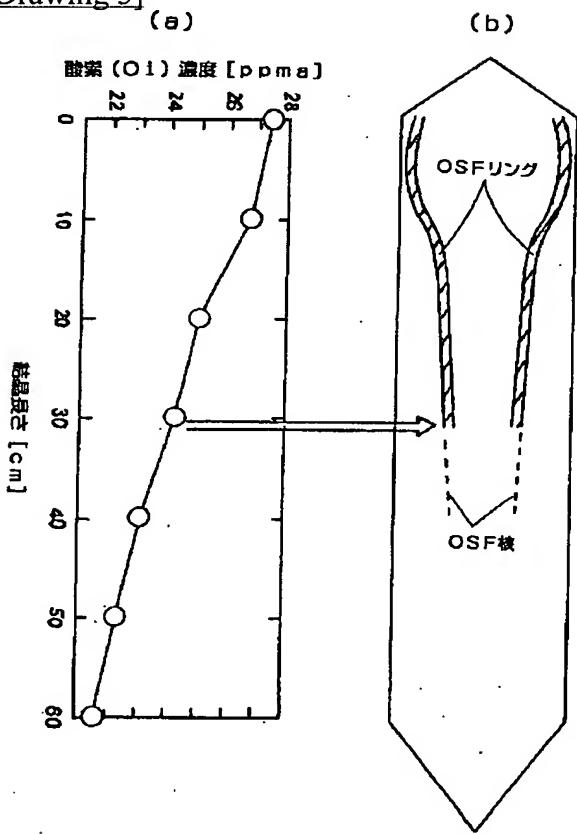
[Drawing 7]

[Translation done.]